Roll No. .....

Total No. of Questions : 07] [Total No. of Pages : 02

BCA (Sem. - 3rd)

COMPUTER SYSTEM ARCHITECTURE

SUBJECT CODE : BC - 403 (N2) (Batch 2K3 Onwards)

Paper ID : [B0226]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.

Section - A

Q1) *(10 × 2 = 20)*

a) What is the difference between trap and interrupt?

b) What must the address field of an indexed addressing mode instruction be to make it the same as a register indirect mode instruction?

c) Differentiate between half adder and full adder?

d) Define OP codes.

e) What is Asynchronous data transfer?

f) Define Seek time.

g) Name the various addressing modes?

h) What is the function of accumulator in 8 bit microprocessor?

i) How pipeline helps in a faster execution of an Instruction?

j) What is mapping process?

Section - B

(4 × 10 = 40)

Q2) (a) List the control functions and micro operations needed for the execution of memory reference instructions.

(b) Discuss the various modes of data transfer.

Q3) (a) Determine the methods to handle branches in a pipeline instruction execution unit.

(b) Explain the interrupt cycle? Draw the flow chart.

Q4) What is a DMA scheme of Data Transfer? Discuss its operating principle. What is cycle stealing mode of data transfer?

Q5) (a) Explain the various page replacement techniques.

(b) What are the various I/O data transfer modes? Differentiate between them?

Q6) (a) Differentiate micro programmed and hardwired control unit?

(b) Discuss the various phases of instruction cycle.

Q7) Explain memory reference instructions in detail.